Electronics - First Opportunity

Question 1

Item	Answer	Comment
1.1	B	
1.2	B	
1.3	B	
1.4	B	
1.5	D	
1.6	A	
1.7	A	
1.8	D	
1.9	B	
1.10	A	
1.11	D	
1.12	C	
1.13	A	
1.14	B & C	identical
1.15	C	

For some questions rough work is necessary:

(1.4) $V_{rms} = \hat{V}/\sqrt{2} = 12/\sqrt{2} \approx 8.49$ V (ans. B).

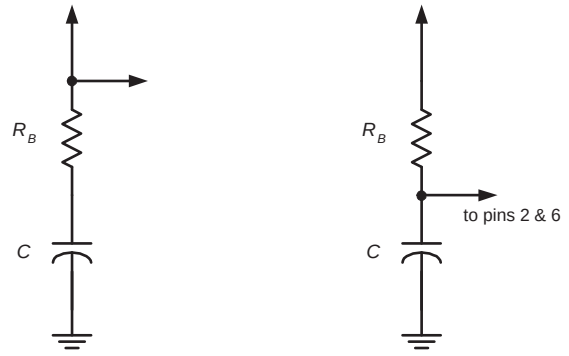
(1.5) Diode is reverse-biased $\Rightarrow$ $I = 0$ mA.

(1.7) $V_{s,rms} = V_{p,rms}/\sqrt{2} = 220/\sqrt{2} \approx 27.5$ V_{rms}. The peak secondary voltage is then $\hat{V}_s = 27.5\sqrt{2} = 38.89$ V. Then assuming silicon diodes and taking away two diode drops leads to $\hat{V}_L = 38.89 - 2(0.7) = 37.49\ V \approx 37.5V$ (ans. B).

(1.9) $V_E = V_B - V_{BE}$ and $I_E = V_E/R_E$; hence $I_E = (6.3 - 0.7)/0.28 = 20$ mA (ans. B).

(1.10) This is an inverting amplifier, hence $A_f = -R_F/R_{IN} = -12.5k/1.5k \approx -8.3$ (ans. A).

(1.11) The circuit in this question is erroneous, either deliberately or otherwise. Best answer is therefore (ans. D).



(a) Erroneous network

(b) Correct network

Figure 1: Question (1.11).

(1.12) Using quotient/remainder theorem $84_{10}/16 = 5$ remainder 4; hence $84_{10} = 54H$ (ans. C).

(1.13) Opposites are $A = \overline{B}$ and $\overline{A} = B$ i.e.

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

. This is the exclusive-OR (XOR) logic gate (ans. A).

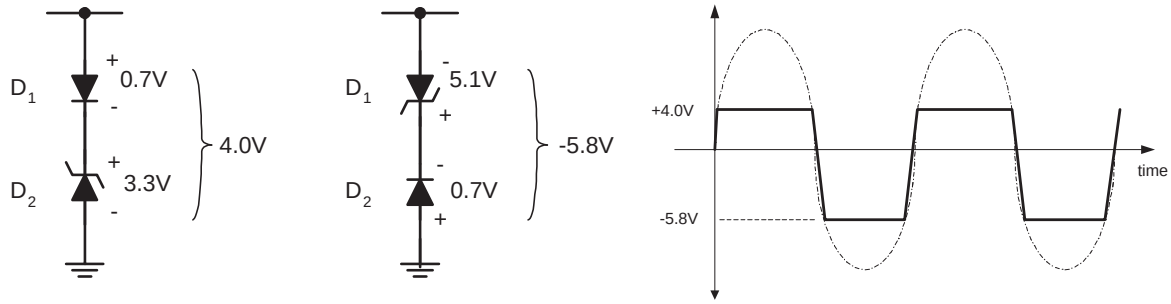
(1.14) $F = A \cdot \overline{B} + \overline{C} + D \cdot E$ (ans. B and ans. C).

(1.15)

$$\begin{aligned} F &= \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot \overline{B} \cdot C \\ &= \overline{A} \cdot \overline{B} \cdot (\overline{C} + C) \\ &= \overline{A} \cdot \overline{B} \cdot 1 \\ &= \overline{A} \cdot \overline{B} \qquad \text{(ans. C)} \end{aligned}$$

Question 2

(2.1) Fig. 2 shows what happens during the input half-cycles.



(a) During the positive half-cycle (b) During the negative half-cycle (c) Output waveform

Figure 2: Zener diode level clippers (not drawn to scale).

(2.2) Given a peak-to-peak ripple of ΔV, it can readily be shown that for a full-wave rectifier

$$C = \frac{I_{dc}T}{\Delta V} \quad \text{where} \quad I_{dc} = \frac{V_{dc}}{R_L} \quad \text{and} \quad T = \frac{1}{2f}.$$

Consequently,

$$R_L = \frac{V_{dc}}{2fC\Delta V} = \frac{12}{2 \times 50 \times 250 \times 10^{-6} \times 0.5} = 960\ \Omega.$$

(2.3) Assume that for an LED that is "ON" the LED voltage drop is approximately +2.0V, and that the optimal LED current is 10 mA; if the circuit is connected to $|\pm 12V|$, then

$$I_R = I_{LED} = \frac{V_{CC} - V_{LED}}{R_L} \quad \Rightarrow \quad R_L = \frac{12-2}{10} = 1\ k\Omega.$$

The circuit is shown in Fig. 3.

Question 3

(3.1) The two KVLs are

$$-V_{CC} + I_B R_B + V_{BE} = 0 \quad (1)$$
$$-V_{CC} + I_C R_C + V_{CE} = 0. \quad (2)$$

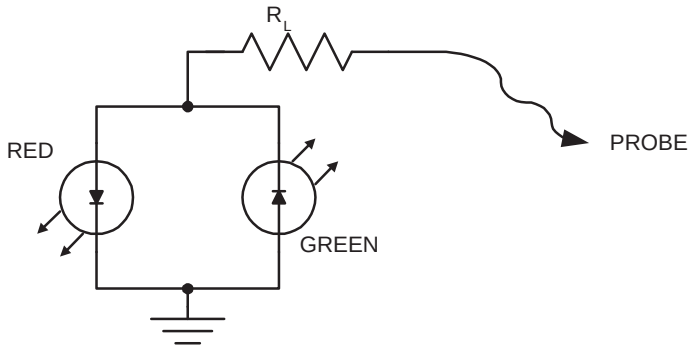


Figure 3: Polarity tester (Q2.3).

Consequently from (1) $I_B = (V_{CC} - V_{BE})/R_B = (10 - 0.7)/232.5 = 0.04$ mA; then $I_{CQ} = \beta I_B = 250 \times 0.04 = 10$mA; therefore from (2), $V_{CEQ} = V_{CC} - I_{CQ}R_C = 10 - 10(0.5) = 5.0V$. The maximum load current is also deduced from (2), i.e. when $V_{CE} = 0$; hence $I_{C,max} = V_{CC}/R_C = 10/0.5 = 20$ mA. The load-line is as shown in Fig. 4.

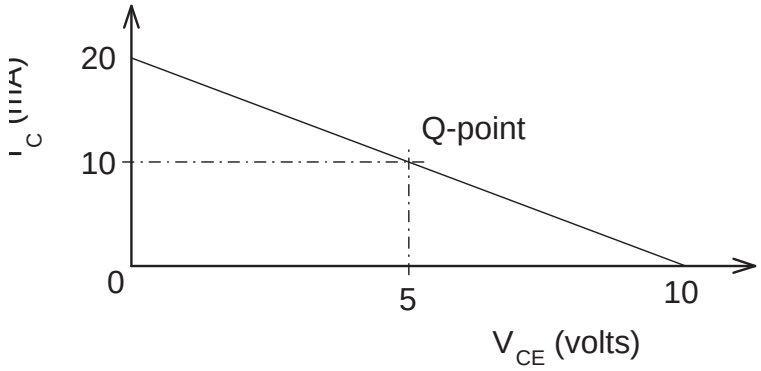


Figure 4: Load-line for (Q3.1).

(3.2) The **TRIAC** is a bi-directional electronic switch that can be triggered into conduction by small bipolar current pulses applied to its gate (G). It has two *anodes*, A1 and A2. The conduction direction is either from

A1 to A2 or from A2 to A1 alternatively. When the triggering pulses fall below a given threshold the conduction ceases. It therefore implements a kind of solid-state alternating current relay.

Typical application: it's main use is in the power-factor correction of a.c. power delivery circuits; other uses are

(a) Light-dimmers

(b) Large (inductive) motor controllers

(c) Energy-efficient lighting controllers, etc.

Question 4

(4.1) Fig. 5 shows the operational amplifier differentiator. The derivation

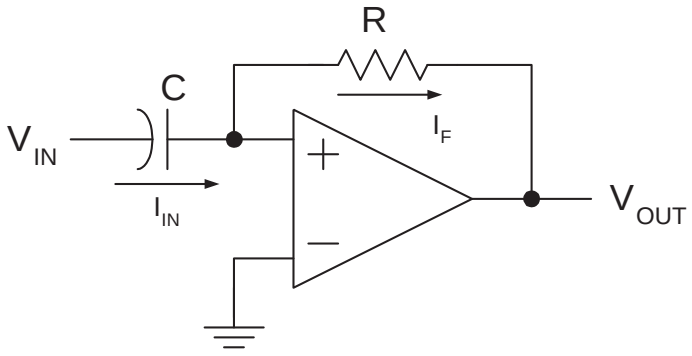


Figure 5: Circuit for (Q4.1).

is as follows: the virtual-earth concept implies that $V^+ = V^- = 0V$. But

$$\begin{aligned} I_{IN} = \frac{dq}{dt} = \frac{d}{dt}(C\Delta V_C)) &= C\frac{d}{dt}\left[V_{IN} - V^-\right] \\ &= C\frac{d}{dt}V_{IN}. \end{aligned} \tag{3}$$

Also,

$$I_F = \frac{V^- - V_{OUT}}{R} = -\frac{V_{OUT}}{R} \tag{4}$$

Equating (3) and (4) since for op-amps $R_{IN} \to \infty$, gives

$$V_{OUT} = -RC\frac{d}{dt}V_{IN}. \tag{5}$$

Equation (5) represents mathematical differentiation, as required.

(4.2) The circuit is a level-comparator with a *current-sink* output. The manner in which the LED is connected indicates that to turn on the LED the op-amp must produce a low-level output. Consequently a high-level output turns the LED off since no potential difference would exist across it in that condition. The comparison level (at V^+) is adjustable, and is set by the 5 $k\Omega$ potentiometer.

Operation: Since $V_O = A_O(V^+ - V^-)$, if $V^- < V^+$, then V_O saturates to $+9V$; whereas if $V^- > V^+$, then the output is at $0V$.

Question 5

(5.1) The circuit is a *monostable* or "one-shot" multivibrator. The timing waveforms are as shown in Fig. 6. It can be shown from first principles

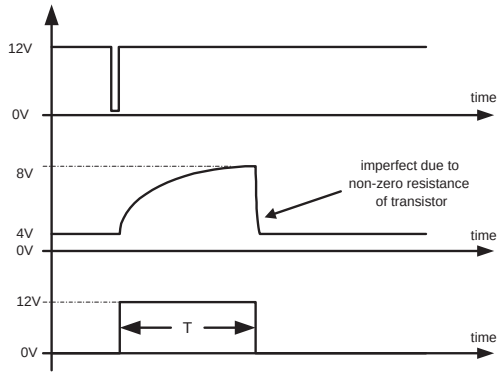


Figure 6: Circuit for (Q5).

that $T = RC\ln 3 \approx 1.09RC$;

Operation: For the sake of brevity I'll leave this out since it is explained in sufficient detail in many texts.

Question 6

(6.1) The circuit given is a *free-running* oscillator or "relaxation" multivibrator. That is, capacitor C charges and discharges alternately. The

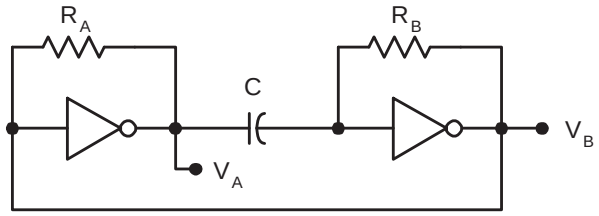


Figure 7: Circuit for (Q6.1).

circuit may be redrawn in terms of inverters only, as shown in Fig. 7; however, since each inverter is connected in a feedback network consisting of a resistor,

Operation: This question is in my view beyond the ability of most electronics students (including the honours) because it necessarily makes use of *hysteresis*. The use of feedback resistors at each inverter means that one the whole the circuit has a voltage hysteresis ΔV_H whose magnitude will depend on the type of inverter used. That is, it will differ for HC (high-speed CMOS/TTL), as well as for LS (low-power Schottky) types. The capacitor then charges through the hysteresis from $V_{OUT,H}$ and discharges from $V_{OUT,H}$ through R_B.

(6.2) This question is contains a fundamental error. The error arise from the fact that any number of things can happen at the inputs of a JK flip-flop (FF) that will guide the progression of the output. This is because a typical FF is a state-machine where even the state itself can be perceived as an input. To illustrate this point consider the absolute truth-table of the JK-FF, shown in Table 1. The role of the clock is to provide an inspection edge that could lead to advancement from state Q_n to state Q_{n+1}. Clearly, until the state of both J and K inputs are specified at a *given* state, it is impossible to derive any waveforms for the circuit.

Table 1: JK-FF truth-table

J	K	Q_n	Q_{n+1}	Condition
0	0	0	0	Memory
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	1	Toggle
1	1	1	0	