Electronics - First Opportunity

Question 1

(Q1.1) Bridge rectifier = full-wave rectifier, with a single transformer output winding

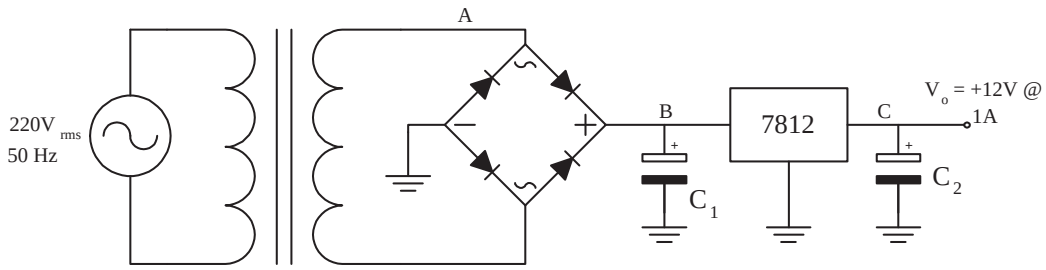


Figure 1: 12 volt regulated bridge rectifier.

The nominal voltage across the 7812 linear regulator is at least 2V, but must not exceed 27V. With respect to the points in Fig. 1 the nominal voltages are: $V_B \geq V_0 + 2V \approx 14V$. This is also the peak voltage across capacitor C_1. The working voltage of C_1 must not be less than $14V$. A minimum of $16V$ is needed. The peak voltage at Point A is two diode drops above point B, i.e. $V_m = V_A = V + B + 2V_D$=14+2(0.7)=15.4V. Hence the secondary rms value is $V_{rms} = V_m/\sqrt{2}$=10.9V$\approx$ 11V. The <u>three</u> recommendations are therefore:

a. the transformer should be about $11V_{rms}$ output;

b. the required transformer step-down ratio is then n=$V_{p,rms}/V_{s,rms}$ =220/11=20;

c. finally, given that the maximum current is foldback limited by the regulator to 1A, the <u>minimum</u> peak power rating of the transformer is $V_m \times I_o = 15.4 \times 1A$=15.4VA.

Choice of capacitor:

For FWR, the output frequency is $f_o = 2f_i$. Assuming a ripple ΔV over a time $\Delta T = T_o$, then

$$I = \frac{dQ}{dT} \approx \frac{\Delta Q}{\Delta T} = C_1 \frac{\Delta V}{\Delta T} \quad \Rightarrow \quad C_1 = \frac{I}{2\Delta V f_i}.$$

Then with $I = 0.2$A, $f_i = 50$Hz,

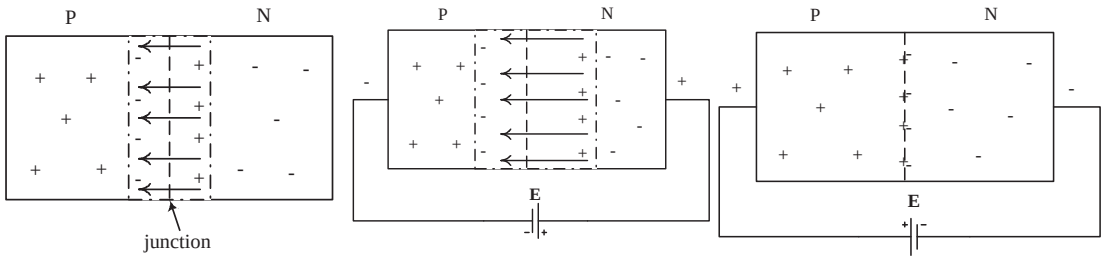
$$C_1 = \frac{0.2}{2 \times 0.45 \times 50}\text{F} = 4444\mu\text{F}.$$

The closest standard value is then 4700μF, 16V (preferably 35V).

(Q1.2a) When a pn junction is formed, electrons and holes diffuse down a concentration gradient. This sets up an internal field where no charges reside - i.e. a region depleted of charge (hence the term "depletion" layer), that is insulating. The potential associated with this force-field opposes further diffusion, Fig. 2(a), and is called the barrier potential, V_ϕ.

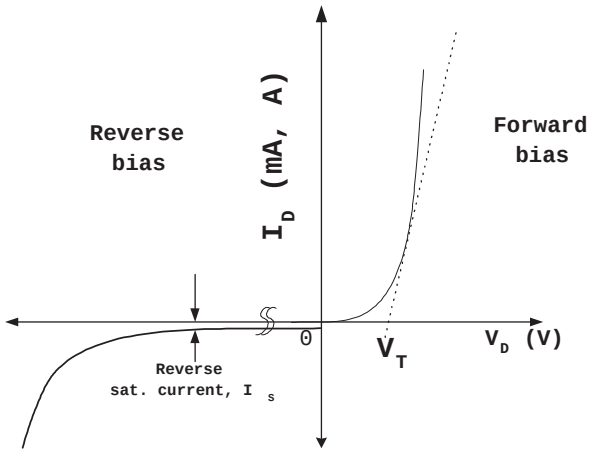
i. in reverse-bias, the polarity of the applied external field reinforces and widens the depletion layer, making the device an even better insulator, Fig. 2(b).

ii. in forward-bias, the polarity of the applied external field neutralizes the internal field, then allows conduction at the point at which the internal field just vanishes, Fig. 2(c).



(a) Internal field (b) Reverse-bias (c) Forward-bias, E=V_ϕ

Figure 2: Biasing the pn-junction.



(Q1.2b)

Figure 3: Typical diode bias characteristics in reverse, forward and breakdown.

Question 2

(2.1) The first KVL equation is:

$$-V_{CC}+I_BR_B+V_{BE}=0 \quad \Rightarrow \quad I_B=\frac{12-V_{BE}}{R_B}=\frac{12-0.7}{330}\frac{(V)}{(k)}=34.24\mu A.$$

Then

$$I_C=\beta I_B \quad \Rightarrow \quad I_C=120\times 0.03424\text{mA}=4.11\text{mA}.$$

The second KVL equation is:

$$-V_{CC}+I_CR_C+V_{CE}=0.$$

(2.2) The load line in Fig. 4 is calculated from the second KVL under the dual conditions: if $I_C=0$ then V_{CE}=maximum, and if $V_{CE}=0$ then I_C=maximum. Hence

$$I_C=0 \quad \Rightarrow \quad V_{CE,max}=12V,$$

and

$$V_{CE}=0 \quad \Rightarrow \quad I_{C,max}=\frac{V_{CC}}{R_C}=\frac{12}{1.2}\text{mA}=10\text{mA}.$$

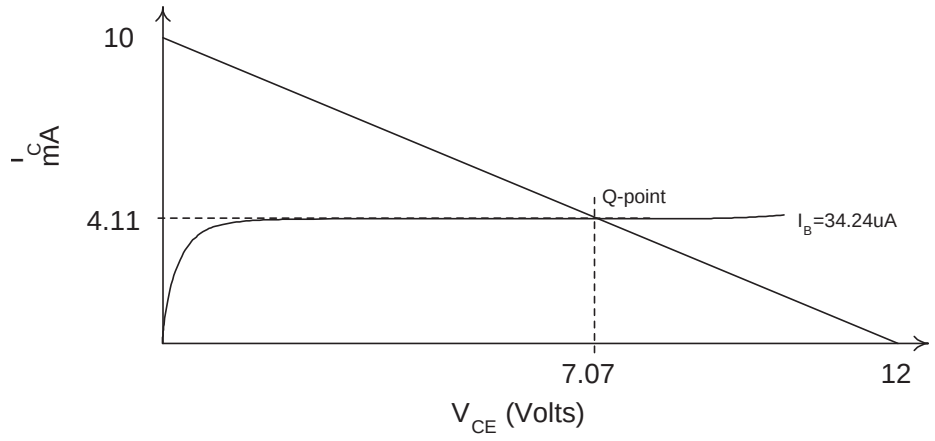


Figure 4: Load line for problem Q2.2.

(2.3) (a) Since R_B is not known, assume that the transistor is overdriven when "ON", and has completely no collector current when "OFF". Therefore it operates at the endpoints of its load line. The output KVL is

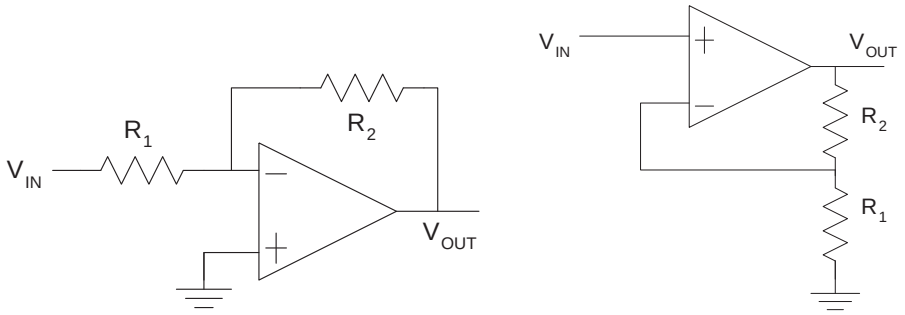
$$-V_{CC}+I_C R_C+V_{CE}=0, \qquad \text{where} \quad V_{CE}=0 \quad \text{when the transistor is "ON".}$$

Hence

$$I_C=\frac{V_{CC}-V_{CE}}{R_{relay}}=\frac{(12-0)V}{75\Omega}=160\text{mA} \quad \Rightarrow \quad I_B=\frac{I_C}{\beta}=\frac{160}{120}=2.133\text{mA}.$$

(b) When V_{BPC}=0V, the transistor is fully "OFF", hence I_C=0mA so that V_{CE}=V_{CC}=12V.

(c) When an inductive load switches ON or OFF, large voltage spikes appear across it as a result of Faraday-Lenz law. Without the diode these spikes would find a path through the transistor. The transistor would then experience a very large reverse voltage across its collector-emitter region and faces the real risk of exceeding its breakdown voltage, with rapid heating and subsequent failure. The diode provides an alternative path for the dissipation of these spikes.



(a) Inverting (b) Non-inverting

Figure 5: Operational amplifiers.

Question 3

(3.1) There are two possible circuits, one inverting and the other non-inverting. These possibilities are shown in Fig. 5. It is easy to show that the closed-loop gain A_f is

$$A_f = -\frac{R_2}{R_1}, \qquad \text{and} \qquad A_f = \left(1 + \frac{R_2}{R_1}\right)$$

respectively for Fig. 5(a) and Fig. 5(b).

(3.2) The circuit is an operational amplifier integrator.

Derivation: By the virtual-earth concept, $V^+ = 0 = V^-$. Also in this case, by KCL $I_{in} = I_F$. Hence

$$\frac{V_{in} - V^-}{R} = I_F = \frac{dq}{dt} = C\frac{d(V^- - V_o)}{dt}$$
$$\Rightarrow \quad \frac{V_{in}}{R} = -C\frac{dV_o}{dt} \quad \Rightarrow \quad V_o = -\frac{1}{RC}\int_{t_0}^{t_1} V_{in}(t)dt.$$

Waveform: Note that the input square-wave pulses (or wave train) are piece-wise contributions of positive and negative constant voltages (say ±E) to the input. Thus when $V_{IN} = +E$,

$$V_O = -\frac{-E}{RC}\int_{t_0}^{t_1} dt = +\frac{E}{RC}t.$$

This represents a straight line with positive gradient (E/RC) passing through the origin. The origin being the initial point of any given

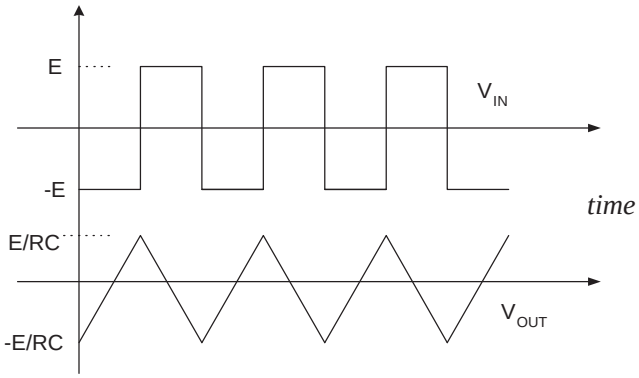


Figure 6: Square to triangular wave converter.

consideration. Similarly, when $V_{IN} = -E$, then

$$V_O = -\frac{E}{RC}\int_{t_0}^{t_1} dt = -\frac{E}{RC}t.$$

This represents a straight line with negative gradient (-E/RC) passing through the particular origin as before. The combined output is then triangular pulse train as in Fig. 6.

Question 4

(4.1) (a) Description of operation can be obtained from many texts. The waveforms at pin 2 and pin 3 are shown in Fig. 7.

(b) In general, a capacitor charges according to the equation

$$V(t) = E(1 - e^{-t/RC})$$

where E is the charging voltage, R is the series resistance and t is time. In the 555-astable circuit, when pin 3 is high, the capacitor is charging from $V_{CC}/3$ to $2V_{CC}/3$ through the effective resistance $(R_1 + R_2)$ connected to a charging source $E = V_{CC}$. In Fig. 7, the repetitive charging time is T_b, where

$$T_c = T_a + T_b \quad \Rightarrow \quad T_b = T_c - T_a.$$

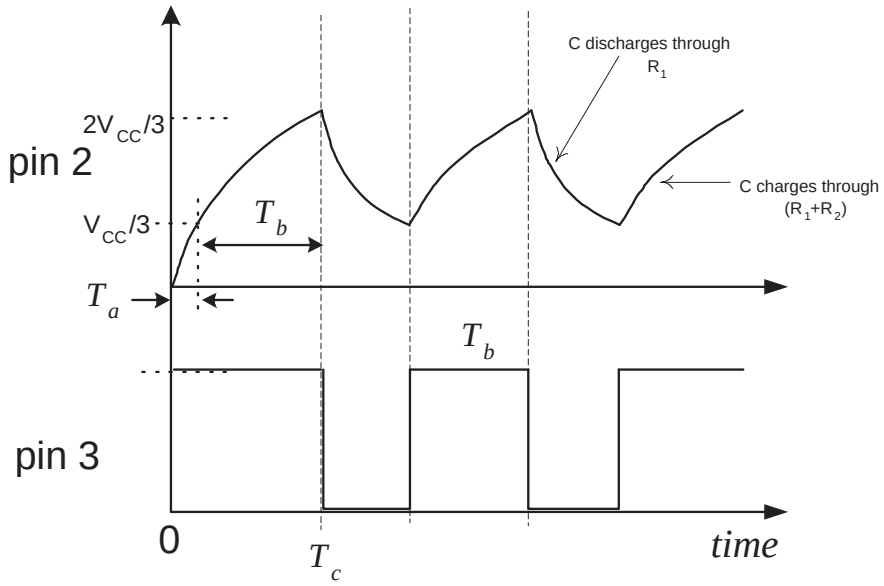


Figure 7: Timing waveforms during charging and discharging.

Then

$$\begin{aligned} \text{for } T_c \quad : \quad & \frac{2V_{CC}}{3} = V_{CC}(1 - e^{-\frac{T_c}{(R_1+R_2)C}}) \\ \Rightarrow \quad & e^{\frac{T_c}{(R_1+R_2)C}} = 3 \\ \Rightarrow \quad & T_c = (R_1 + R_2)C \ln 3. \end{aligned}$$

similarly,

$$\begin{aligned} \text{for } T_a \quad : \quad & \frac{2V_{CC}}{3} = V_{CC}(1 - e^{-\frac{T_a}{(R_1+R_2)C}}) \\ \Rightarrow \quad & e^{\frac{T_a}{(R_1+R_2)C}} = \frac{3}{2} \\ \Rightarrow \quad & T_a = (R_1 + R_2)C \ln \frac{3}{2}. \end{aligned}$$

Hence

$$\begin{aligned} T_b = T_c - T_a &= (R_1 + R_2)C(\ln 3 - \ln \frac{3}{2}) \\ &= (R_1 + R_2)C \ln \frac{3}{3/2} \\ &= (R_1 + R_2)C \ln 2. \end{aligned}$$

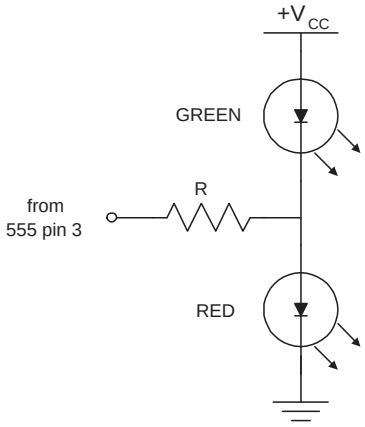


Figure 8: Current sink/source LED driver addition.

(c) The 555-timer is operated in both current sink (active LOW output) and current source (active HIGH output) mode.
The KVL of the LED driver (in either mode) is:

$$-V_{CC} + V_{LED} + I_R R = 0$$

where I_R=I_{LED} is the nominal LED current, and typically for most LEDs, $V_{LED} \approx 2.0$V and $I_{LED} \approx 10$mA. Hence

$$R = \frac{V_{CC} - V_{LED}}{I_R} \approx \frac{9-2}{10} = 0.7k\Omega.$$

A standard 680Ω resistor would suffice.
The circuit is shown in Fig. 8.

Question 5

(5.1) The circuit that implements the logic function

$$F = \overline{A \cdot \overline{B} + \overline{B} \cdot C} + D \cdot E$$

is shown in Fig. 9.

(5.2) The circuit is a set-reset (SR) FF made out of NOR gates.
Table 1 leads to the answer in Table

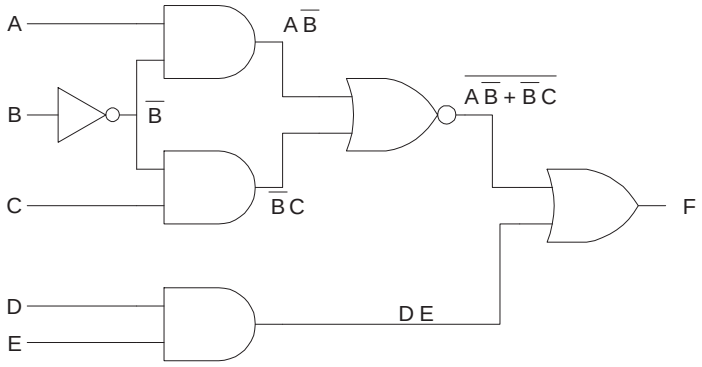


Figure 9: Logic circuit implementation for (Q5.1).

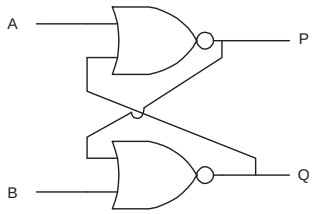


Figure 10: The redrawn circuit.

S	R	Q_n	Q_{n+1}	$P = \bar{Q}_{n+1}$	Condition
0	0	0	0	1	Memory
0	0	1	0	1	”
0	1	0	1	0	Set
0	1	1	1	0	”
1	0	0	0	1	Reset
1	0	1	0	1	”
1	1	0	0	0	Not allowed
1	1	1	0	0	”

Table 1: Truth-table of the NOR gate SR flip flop in Fig. 10.

A	B	Q	Condition
0	0	0	↙ memory
0	1	0	↙ set
0	0	1	↙ memory
1	0	1	↙ Reset
0	0	0	↙ memory
0	1	0	↙ set
		1	

Table 2: Answer to Problem 5.2

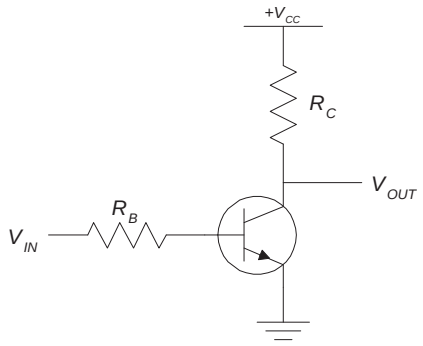


Figure 11: NOT gate using a bipolar junction transistor.

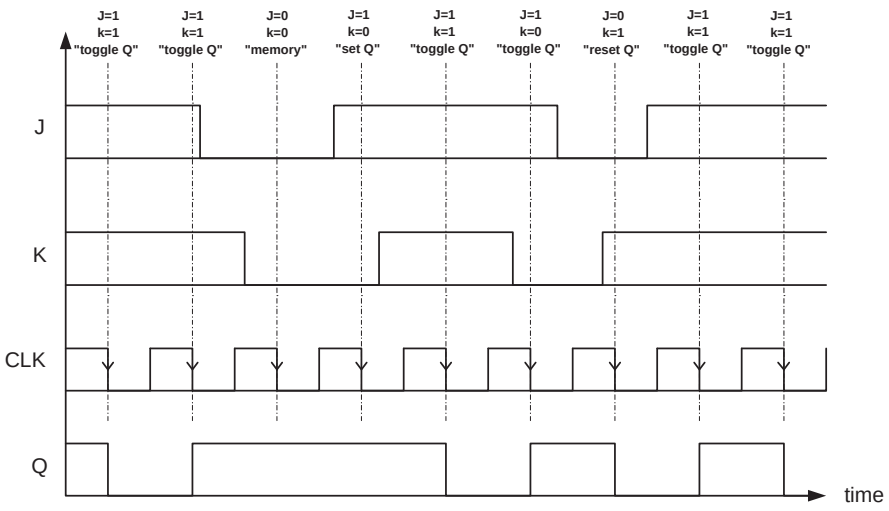


Figure 12: Typical waveform in a negative going transition JK flip flop. The initial state assumed as Q="1".

(5.3) An inverter using a BJT is shown in Fig. 11.

(5.4) The question needed to have the state of the JK inputs as well as the initial state of the flip flop specified to be answered correctly. A typical set of waveforms might be as shown in Fig. 12. The truth-table of the clocked JK-FF is shown in Table 3.

Table 3: JK-FF truth-table

J	K	Q_n	Q_{n+1}	Condition
0	0	0	0	Memory
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	1	Toggle
1	1	1	0	

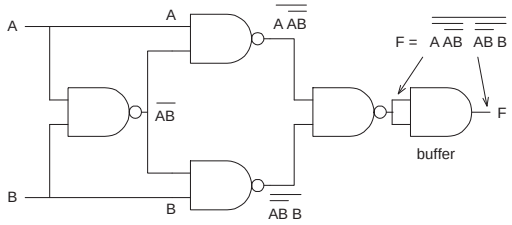


Figure 13: Building the equation of F.

(5.5) The logic function: Following through Fig. 13 gives

$$\begin{aligned}
F &= \overline{\overline{A\overline{AB}} \cdot \overline{\overline{AB}B}} \\
&= \overline{\overline{A(\bar{A}+\bar{B})} \cdot \overline{B(\bar{A}+\bar{B})}} \\
&= \overline{\overline{A\bar{A}+A\bar{B}} \cdot \overline{\bar{A}B+B\bar{B}}} \\
&= \overline{\overline{0+A\bar{B}} \cdot \overline{\bar{A}B+0}} \\
&= \overline{\overline{A\bar{B}} \cdot \overline{\bar{A}B}} \\
&= \overline{(\bar{A}+B) \cdot (A+\bar{B})} \\
&= \overline{\bar{A}A+\bar{A}B+AB+B\bar{B}} \\
&= \overline{0+\bar{A}B+AB+0} \\
&= \overline{\bar{A}B+AB} \\
&= \overline{\bar{A}B} \cdot \overline{AB} \\
&= (A+B) \cdot (\bar{A}+\bar{B}) \\
&= A\bar{A}+A\bar{B}+\bar{A}B+B\bar{B} \\
&= A\bar{B}+\bar{A}B \\
\Rightarrow F &= A \oplus B \qquad \text{(simplification)}
\end{aligned}$$

This represents the exclusive-OR (XOR) function.

(5.6) The circuit can only work with CMOS type gates, and the question needed to specify this fact. The general objective is to show that since the CMOS gate is a metal-oxide device, its "gate" draws no output, such that for a suitably chosen resistor in feedback configuration in Fig. 14, the nominal bias point will be set at $V_{CC}/2 \approx 5/2 = 2.5$V. The particular circuit is well known for being notoriously difficult to start-up and is therefore considered generally unreliable. None the

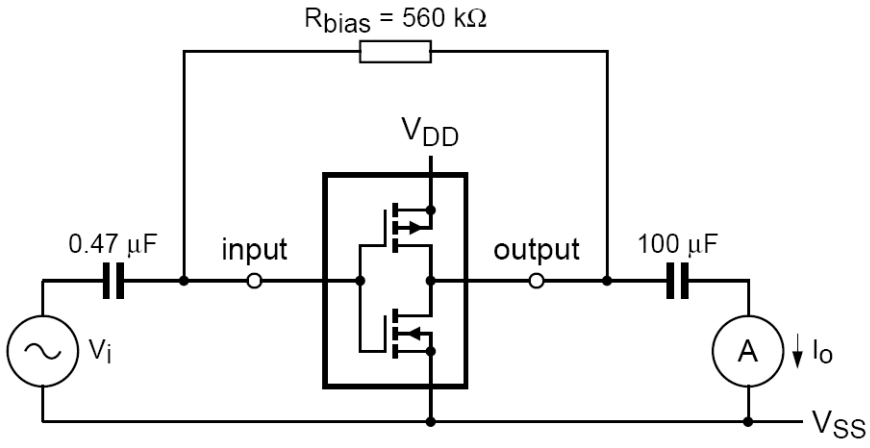


Figure 14: Transfer characteristic of the unbuffered CMOS NOT gate.

less, each amplifier has a transconductance given by

$$g_{fs} = \left.\frac{dI_o}{dV_I}\right|_{V_o}.$$

Assuming that the relaxation occurs at the extremes of output then the oscillator in question has a capacitor that relaxes from V_{CC} to $V_{CC}/2$ repetitively. My impression is still that such questions strain the student unduely.

Obama for President!